J Solid State Electrochem (2000) 4: 125–130

ORIGINAL PAPER

Manabu Itsumi · Shin-ichi Ohfuji · Hideo Akiya
Satoshi Nakayama · Hideo Yoshino

Electrical characteristics of silicon-nodule-related via failures observed in aluminum-silicon interconnects

Received: 22 February 1999 / Accepted: 30 June 1999

Abstract We have evaluated the electrical characteristics of silicon-nodule-related via failures in the aluminum interconnects of silicon integrated circuits. Current-voltage measurements indicated that the conduction mechanism follows Ohm's law. The resistance was 1.5–3 kΩ for a silicon nodule at a via of 1.0 μm × 1.0 μm. When the applied voltage was 3–6 V, the resistance decreased abruptly. This transition (abrupt decrease in resistance) was irreversible. We think that the resistance of 1.5–3 kΩ and the transition voltage of 3–6 V are two factors characterizing the silicon nodule. We can explain these values by assuming that aluminum in the silicon nodules at a solubility limit concentration acts as an acceptor.

Key words Via failures · Silicon nodules · Aluminum interconnects

Introduction

Via-hole contact failures in metal interconnects are one of the most important problems affecting production yields and the reliability of silicon (Si) integrated circuits (ICs). The major causes of via failures in the 1980s, when Si-containing aluminum [Al(Si)] interconnects were used, were insufficient cleaning of vias [1] or the presence of Si nodules [2–4] at the vias. In the 1990s, when Al(Cu) interconnects [5, 6], tungsten vias [7, 8], and barrier metal layers [9, 10] were used, failures occurred because of $TiN/TiSi_2$ interface reaction [9], via delamination [11], or void formation [8, 12].

Recently, a proposed Al(Si) plug structure [13] for via holes with a diameter of 0.1–0.18 μm and with aspect ratio of 7–10 has attracted much attention for possible use in future sub-quarter-micron ICs. In addition, Al(Si) is widely used for metal interconnects in poly-Si thin-film transistors (TFTs) [14–16] and the peripheral circuits of liquid-crystal displays (LCDs) [16], which are increasingly used in various multimedia products. This is because it is suitable for wet etching, which makes defining interconnects easy. It is also used for metal interconnects in ball semiconductors [17], which are attracting a lot of interest. Furthermore, Al(Si) is still used as a control [18] when various interconnect materials are compared. For these reasons, Si nodules remain an important problem affecting via failures of Al(Si) interconnects.

The size of a Si nodule, the generation probability of Si-nodule-related via failures, and the dependence of failures on nodule development have been investigated by several researchers [2–4]. It has also been reported that the maximum size of a Si nodule is 0.9–1.2 μm; however, the electrical properties of Si nodules are not fully understood. More quantitative characterization of them is needed to properly analyze via failures.

We characterize Si nodules by examining their electrical resistance and the abrupt changes in the resistance at a specific voltage. This, in effect, means examining the resistance of poly-Si-containing Al at a solubility limit concentration.

M. Itsumi (✉)
NTT Lifestyle and Environmental Technology Laboratories,
Atsugi-shi, Kanagawa 243-0198, Japan

S. Ohfuji
NTT Lifestyle and Environmental Technology Laboratories,
Musashino, Tokyo 180-8585, Japan

H. Akiya
NTT Science and Core Technology Laboratory Group,
Atsugi-shi, Kanagawa 243-0198, Japan

S. Nakayama
NTT Telecommunications Energy Technology Laboratories,
Atsugi-shi, Kanagawa 243-0198, Japan

H. Yoshino
NTT Electronics Corporation, Atsugi-shi,
Kanagawa 243-0198, Japan

Experimental

Sample preparation

The samples we used had via chain patterns that were composed of two layers of Al interconnects as shown in Fig. 1. Al interconnect 1 (Al 1) had a width of 0.8 μm and a thickness of 0.5 μm. Al interconnect 2 (Al 2) had a width of 2.0 μm and a thickness of 1.0 μm. The via holes were 1.0 μm × 1.0 μm. There were 500 vias in a chain, 1200 via chains in a wafer, and 24 wafers in a fabrication lot. We fabricated 25 lots for this study. The concentration of silicon in the aluminum was 2%.

The fabrication process used for complementary metal-oxide-silicon (CMOS) LSIs with a two-level interconnect was used for sample preparation. The silicon wafers were 4-inch-diameter Czochralski silicon with (100) orientation. The gate oxide thickness was 15 nm and gate length was 0.8 μm. The gate material was phosphorus-doped poly-Si for the p-channel and n-channel MOS transistors. Subsequent to the chemical vapor deposition of SiO_2 and boron-phosphorus silicate glass films, photolithography and dry etching were used to make the contact holes. Then Al 1 was formed on the silicate glass. Silicon dioxide films were deposited using a bias-sputter apparatus. This was followed by via hole formation, a pre-etching processes, and deposition of Al 2. Finally, post-metallization annealing at 400 °C in H_2/N_2 for 30 min was done prior to measurement.

Measurement

The electrical resistance of the via chains throughout the wafers was measured with an automatic measurement system. Current-voltage (*I-V*) characteristics of via chains with a large resistance (i.e. failures detected) were measured.

Some samples were then repeatedly subjected to post-metallization annealing (at 400 °C in H_2/N_2 for 30 min) to determine whether the additional annealing increased or decreased the probability of via failures.

Results

Current-voltage characteristics

The current-voltage characteristics of via chains without failures indicated that the conduction mechanism was ohmic and the resistance was about 100 Ω.

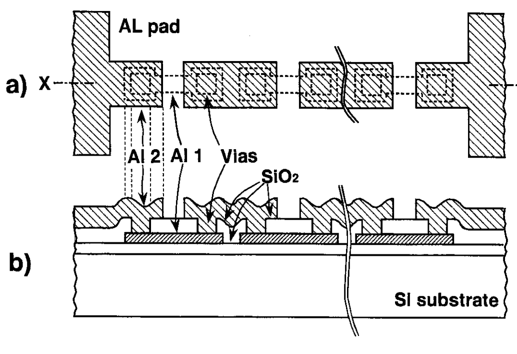

Fig. 1 A schematic illustration of the Al interconnect chains used for electrical measurement: **a** plan view; **b** cross-sectional view along *X-X'* in **a**. Al 2 (width 2 μm, thickness 1 μm) was connected to Al 1 (width 0.8 μm, thickness 0.5 μm) through a via (square with 1 μm sides). The number of vias in a chain was 500

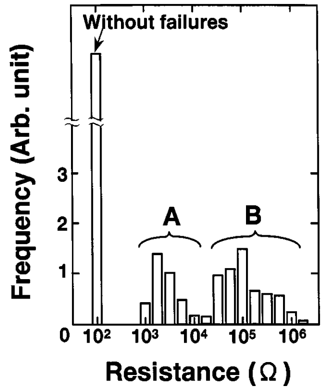

Fig. 2 Histogram for resistance of chains. Failures were classified into two groups: group A was related to Si nodules and is the main theme of this paper; group B depended on via-hole cleaning and was due to a thin oxide layer at the hole

Figure 2 is a histogram for the resistance of the via chains we fabricated. Almost all the chains had a resistance of about 100 Ω and they were free of failures. There were two groups of failures with different distributions of resistance: the first had a resistance from 10^3 to 10^4 Ω (group A in Fig. 2), and the second had a resistance from 3×10^4 to 1×10^6 Ω (group B in Fig. 2).

Group B was closely related to the via hole cleaning procedure and this may be due to an unintentionally formed thin oxide layer between Al 1 and Al 2. However, group A was related to Si nodules at a via.

Figure 3 shows an example of the current-voltage characteristics of via chains with this failure. The slope of current versus applied voltage is almost straight and only a little curved, which seems to suggest that the conduction mechanism is close to ohmic. As this figure shows, the resistance is, roughly speaking, constant and about 1.6×10^3 Ω, although, strictly speaking, it decreases gradually with increasing applied voltage.

The approximately straight slope of current versus voltage, shown in Fig. 3, suggests that the origin of the failure is not related to the thin oxide layer between Al 1 and Al 2. This is because the conduction mechanism through the thin oxide layer generally has exponential-type current-voltage characteristics.

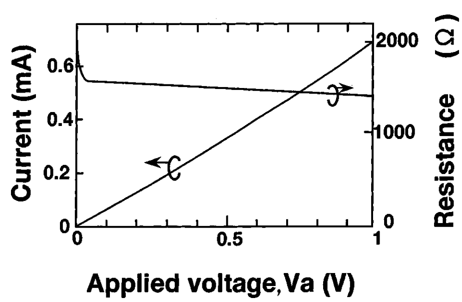

Fig. 3 Current-voltage (*I-V*) characteristics of a chain with failures in group A. The resistance was about 1.5×10^3 Ω

Effect of repeated post-metallization annealing

The probability of via-hole failures increased monotonically with the number of post-metallization annealing treatments. The dependence of the via-hole failures on resistance is shown in Fig. 4a. These failures are characterized by a peak in the resistance at about $2 \times 10^3\ \Omega$.

The relationship between resistance before additional annealing and the change in resistance with additional annealing is shown in Fig. 4b. In detail, when the resistance before additional annealing is smaller than $2 \times 10^3\ \Omega$, additional annealing increases the resistance slightly. When the resistance before additional annealing is larger than $3 \times 10^3\ \Omega$, additional annealing reduces the resistance slightly. This is an interesting phenomenon. We think that the smaller Si nodules become larger and the larger Si nodules become smaller toward an optimum (i.e. the most stable) state, shape, or size fitting the via-hole structure. This mechanism deserves further study.

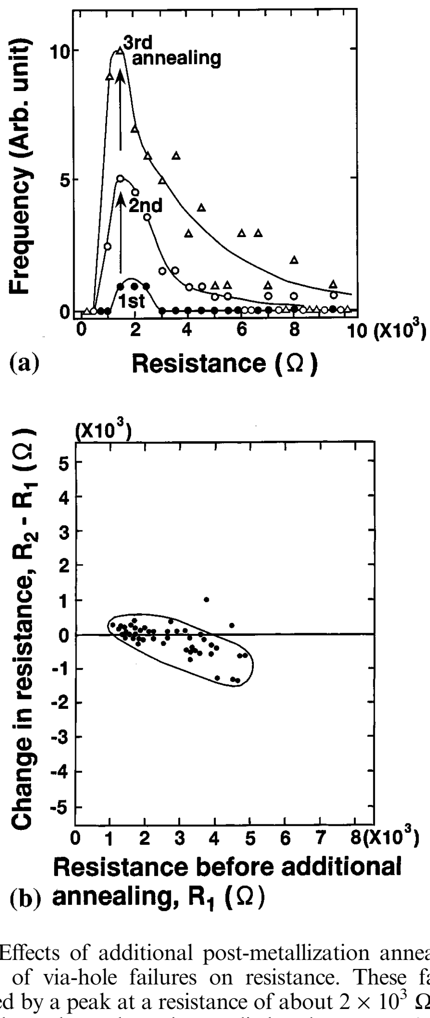

Fig. 4a, b Effects of additional post-metallization annealing. **a** The dependence of via-hole failures on resistance. These failures were characterized by a peak at a resistance of about $2 \times 10^3\ \Omega$. Resistance was defined as that when the applied voltage was 0.1 V. **b** The relationship between resistance before additional annealing and the change in resistance with additional annealing

At any rate, via failures with Si nodules are characterized by a peak in the resistance at about $2 \times 10^3\ \Omega$ for the present experimental conditions.

Abrupt breakdown of via failures

When the voltage applied to via chains with failures is smaller than 2 V, the current-voltage characteristics in Fig. 3 are maintained even if the measurement is repeated many times. When the applied voltage exceeds a certain value, however, the current increased abruptly, which is indicated by T in Fig. 5a. In this figure, when the applied voltage reaches a value of 3.85 V, the current jumps from 3 to 38.5 mA. Thereafter, when the applied voltage is decreased, the current decreases along the line denoted by S in the figure. When the applied voltage is increased again, the current-voltage characteristics follow the line denoted by S′ (which is substantially the same as S) in the figure. That is, the current jump at a voltage of 3.85 V is irreversible. The current-voltage characteristics of S (or S′) correspond to a resistance of 100 Ω, which is equal to the resistance of via chains without failures. This means that the failure was repaired when the current jumped and that normal conduction in the via chain was attained. For convenience, here, the applied voltage causing the current jump is called the transition voltage.

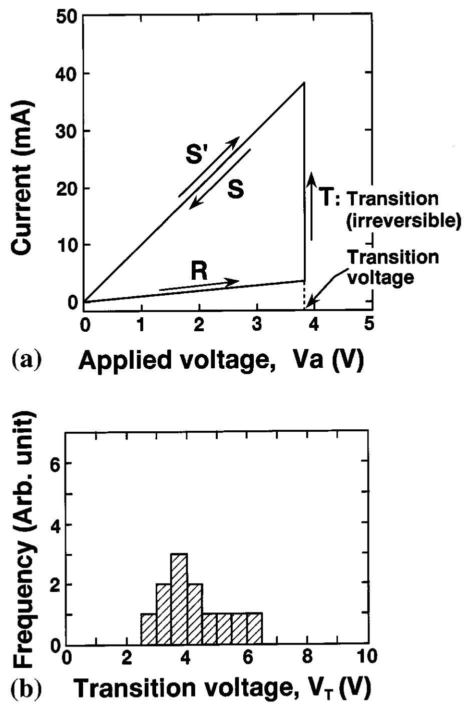

Fig. 5a, b Irreversible current jump (transition) at various applied voltages. **a** Current-voltage characteristics explaining the irreversible current jump (transition) at some applied voltages. **b** Histogram for transition voltage

Figure 5b is a histogram of the transition voltage. It can be seen that the transition voltage ranges from 2.5 to 6.5 V, which will lead us to an important parameter to find the breakdown mechanism involved.

Discussion

Figure 6 is a schematic diagram of a model for the via-hole failure we dealt with. We assumed that Si nodules of about 1 μm are situated at a via hole and act as resistance between Al 1 and Al 2. We also assumed that the Si nodules contain Al atoms at solid solubility level. Onoda and colleagues [19] observed the electron diffraction pattern of a Si nodule and suggested that the Si nodule is polycrystalline with large grains. Under these assumptions and Onoda and colleagues' conclusion, we estimated the resistance and breakdown voltage of a Si nodule.

The concentration of Al atoms in a Si nodule is estimated to be about 3×10^{18} atoms/cm^3, from the extrapolation of data in Fig. 7. If these Al atoms in Si are fully activated at 400 °C and they act as an acceptor, the concentration of 3×10^{18} atoms/cm^3 will lead to a resistivity of about 0.15 Ω cm, which was estimated from the data for boron (as an acceptor) in Fig. 8 (although the dopant and process conditions are different).

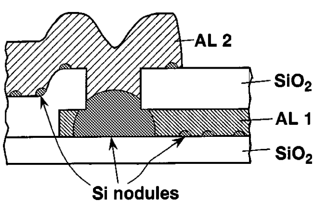

Fig. 6 A schematic illustration of Si nodules as the origin of via-hole failures. Silicon nodules situated at via holes act as resistance between Al 1 and Al 2

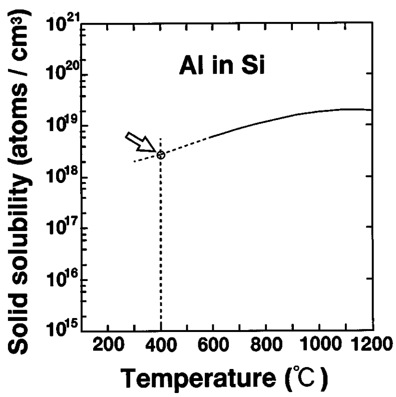

Fig. 7 Solid solubility of Al in Si as a function of temperature (data from Trumbore [20]. The solid solubility of Al in Si at 400 °C is estimated to be 3×10^{18} atoms/cm^3 (indicated by *arrow*), obtained from extrapolation of the data at temperatures higher than 550 °C

The resistance of the via failure, R, can be given using the following equation:

$$R = rL/S \tag{1}$$

where r is the resistivity, L is the effective length of the Si nodule along the electronic current, and S is an effective cross-section of the Si nodule perpendicular to the current. Assuming that L is typically 1 μm and S is also typically 1 μm^2, we obtain

$$R = 0.15\ \Omega\ \text{cm} \times 1\ \mu\text{m}/1\ \mu\text{m}^2 = 1.5 \times 10^3\ \Omega \tag{2}$$

which agrees approximately with the experimental results in Fig. 5b.

The transition voltage of poly-Si with a resistivity of 0.15 Ω cm is estimated to be about 2 V from extrapolation of the data in Fig. 9. This is a very rough ex-

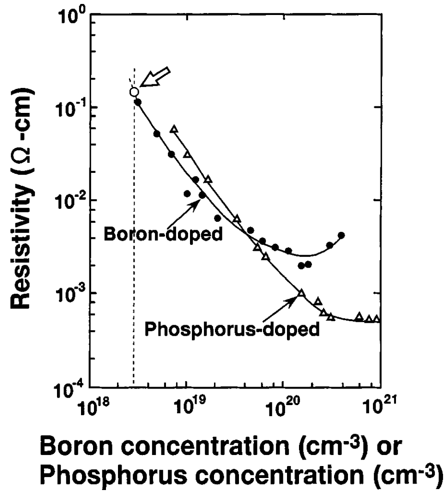

Fig. 8 The dependence of poly-Si resistivity on impurity concentration (data from Nakayama et al. [21]). Boron in Si acts as an acceptor and phosphorus in Si acts as a donor. Resistivity of poly-Si with acceptors at a concentration of 3×10^{18} atoms/cm^3 is estimated to be about 0.15 Ω cm (indicated by an *arrow*), obtained from extrapolation of the data

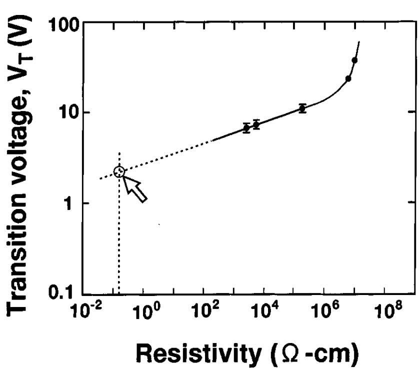

Fig. 9 The dependence of transition voltage on poly-Si resistivity. (data from Tanimoto et al. [22]. *Solid circles* represent poly-Si films with a thickness of 1 μm and the impurity in the poly-Si is arsenic. Resistivity of 0.15 Ω cm leads to a transition voltage of about 2 V, (indicated by *arrow*), obtained from extrapolation of the data

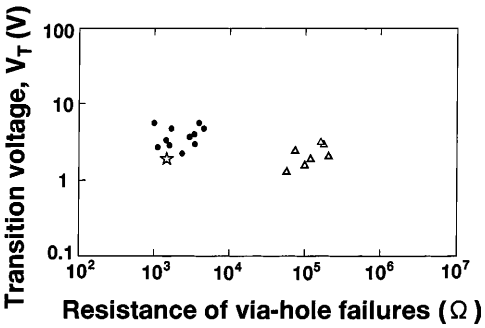

Fig. 10 The relationship between transition voltage and resistance of via-hole failures. *Solid circles* represent data related to Si nodules. The *open star* is a calculated value derived from Figs. 7, 8, and 9. *Open triangles* represent data related to via-hole cleaning, or to a thin oxide layer unintentionally formed between Al 1 and Al 2

trapolation, but this value agrees with the experimental results in Fig. 5b, at least as an order estimate.

A comparison between a set of resistances and transition voltages was derived from Eq. 2 and Fig. 9, and the experimental results are shown in Fig. 10. The good agreement in the figure suggests that the model described above is generally reasonable.

In addition, as a mechanism for transition, we assume the following model. When the applied voltage reaches a transition voltage, the corresponding electric current leads to an increase in local joule-heat of up to several hundred degrees centigrade, excessively activating the Al atoms and, finally, inducing a spiking of aluminum atoms into the Si nodule. This spiking might become a conductive path in the Si nodule. This model is only speculative and should be studied further.

Conclusion

The current-voltage characteristics of via-hole failures related to Si nodules indicated that the conduction mechanism was approximately ohmic. The electrical resistance of the failures was characterized as 1.5–3×10^3 Ω. The applied voltage that caused the abrupt decrease in the resistance ranged from 3 to 6 V. These results suggest that the origin of the failures was silicon nodules formed during heat treatment. These electrical characterizations can be explained in terms of the electrical characterization of poly-Si-containing Al.

Acknowledgements We are indebted to Dr. Noboru Shiono of the Electronics Reliability Center of Japan and Mr. Takemi Ueki of NTT Electronics Corporation for their help in the long-term reliability testing of the aluminum interconnects and via holes. We also wish to thank Dr. Kouhei Ehara of NTT Electronics Corporation and Dr. Kazumitsu Yasuda for their comments on the experimental conditions for aluminum interconnect formation. We would also like to thank Dr. Masafumi Tanimoto for his comments about the dependence of transition voltage on poly-Si film thickness. We are grateful for Dr. Eisuke Arai of the Nagoya Institute of Technology and Dr. Susumu Muramoto of NTT Electronics Corporation for their continued encouragement throughout the research.

References

1. Tomioka H, Tanabe S, Mizukami K (1989) A new reliability problem associated with Ar ion sputter cleaning of interconnect vias. In: IEEE 27th annual international reliability physics symposium. The Institute of Electrical and Electronic Engineers, Inc., Phoenix, Arisona, April 1989, p 53
2. Tatsuzawa T, Madokoro S, Hagiwara S (1985) Si nodule formation in Al-Si metallization. In: IEEE 23rd annual international reliability physics symposium. The Institute of Electrical and Electronic Engineers, Inc., Orlando, Florida, March 1985, p 138
3. Yamada Y, Isobe A, Takao S (1986) In: Extended abstracts 47th autumn meeting, Japanese Society of Applied Physics, 29p-N-12, p 504 (in Japanese)
4. Yamaha T, Fujioka T, Hanagasaki O, Sato H, Hotta T (1990) Non-Ohmic via contacts caused by Si nodules from WSix barrier. In: Abstracts 37th spring meeting. Japanese Society of Applied Physics, 28p-ZA-4, p 558 (in Japanese)
5. Yeo I-S, Ho PS (1996) Stress relaxation and microstructural change in passivated Al(Cu) lines. In: IEEE 34th international reliability physics proceedings. The Institute of Electrical and Electronic Engineers, Inc., Dallas, Texas, April 1996, p 131
6. Hosaka M, Kouno T, Hayakawa Y, Niwa H, Yammada M (1998) Ti layer thickness dependence on electromigration performance of Ti/AlCu metallization. In: IEEE 36th international reliability physics proceedings. The Institute of Electrical and Electronic Engineers, Inc., Reno, Nevada, March 1998, p 329
7. Sekiguchi M, Yamanaka M, Mayumi S (1997) Effect of Al-W intermetallic compounds on electromigration in Al/CVD-W interconnects. In: IEEE 35th international reliability physics proceedings. The Institute of Electrical and Electronic Engineers, Inc., Denver, Colorada, April 1997, p 221
8. Liang V, Sur H, Bothra S (1998) Passive voltage contrast technique for rapid in-line characterization and failure isolation during development of deep submicron ASIC CMOS technology. In: Proceedings 24th international symposium for testing and failure analysis. ASM International, Dallas, Texas, p 221
9. Banerjee K, Amerasekera A, Dixit G, Cheung N, Hu C (1997) Characterization of contact and via failure under short duration high pulsed current stress. In: IEEE 35th international reliability physics proceedings. The Institute of Electrical and Electronic Engineers, Inc., Denver, Colorada, April 1997, p 216
10. Yoshida T, Hashimoto S, Hosokawa H, Ohwaki T, Mitsushima Y, Taga Y (1997) Influence of water absorption of dielectric underlayers on Al(111) crystallographic orientation in Al-Si-Cu/Ti/TiN/Ti layered structures. In: IEEE 35th international reliability physics proceedings. The Institute of Electrical and Electronic Engineers, Inc., Denver, Colorado, April 1997, p 226
11. Lee YH, Wu K, Mielke N, Ma LJ, Hui S (1997) Via delamination – a novel electromigration failure mechanism. In: IEEE 35th international reliability physics proceedings. The Institute of Electrical and Electronic Engineers, Inc., Denver, Colorado, April 1997, IEEE, p 206
12. Domae S, Masuda H, Tateiwa K, Kato Y, Fujimoto M (1998) Stress-induced voiding in stacked tungsten via structure. In: IEEE 36th international reliability physics proceedings. The Institute of Electrical and Electronic Engineers, Inc., Reno, Nevada, March 1998, p 318
13. Horie H, Imai M, Itoh A, Arimoto Y (1996) Novel high aspect ratio aluminium plug for Logic/DRAM LSIs using polysilicon aluminum substitute (PAS). In: Technical digest of IEEE international electron devices meeting. Institute of Electrical and Electronic Engineers, Inc., San Francisco, December 1996, p 946
14. Wang YZ, Awadelkarim OO (1998) Microelectron Reliab 38: 1835
15. Kim K-J, Kim O (1997) J Electrochem Soc 144: 2501
16. Fa C, Chen T-J, Jeng J-N (1997) J Electrochem Soc 144: 3645

17. Yamashita M, Takeda N (1998) Denshi Zairyo 37 (11): 21
18. Tao J, Chen JF, Cheung NW, Hu C (1996) Electromigration design rules for bidirectional current. In: IEEE 34th international reliability physics proceedings. The Institute of Electrical and Electronic Engineers, Inc., Dallas, Texas, April 1996, p 180
19. Onoda H, Umemura E, Madokoro S (1987) Technical report of The Institute of Electronics, Information and Communication Engineers, SDM 87–70. IEICE, p 49 (in Japanese)
20. Trumbore FA (1960) Bell System Tech J 39: 205
21. Nakayama S, Kawashima I, Murota J (1986) J Electrochem Soc 133: 1721
22. Tanimoto M, Murota J, Ohmori Y, Ieda N (1980) IEEE Trans Electron Devices 27: 517